In the Claims

Please amend the claims as shown below.

1. (Canceled)

2. (Currently amended) The method of claim [[1]] 33, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip.

3. (Currently amended) The method of claim [[1]] 33, wherein the plurality of submodules comprise a memory module and a Digital Signal Processor (DSP) core.

4. (Currently amended) The method of claim [[1]] 33, wherein instantiation constraints are used to select the plurality of submodules.

5. (Currently amended) The method of claim [[1]] 33, wherein the design automation tool is a synthesis or a place and route tool.

6. (Canceled)

7. (Currently amended) The method of claim [[6]] 33, further comprising identifying a plurality of inputs, wherein the inputs identified comprise the input pins of the ~~top-level~~ module, one of the output lines of one of the parameterized submodules ~~output lines~~, and registers.

8. (Currently amended) The method of claim [[6]] 7, further comprising identifying a plurality of outputs, wherein the outputs identified comprise the output pins of the ~~top-level~~ module, one of the input lines of one of the parameterized submodules ~~input lines~~, and registers.

9. (Currently amended) The method of claim 8, ~~wherein providing logic to interconnect the plurality of parameterized submodules~~ further ~~comprises~~ comprising classifying the inputs and outputs identified as clock lines, control lines, and data lines.

10-12. (Canceled)

13. (Currently amended) The method of claim [[6]] 33, wherein parameterizing the plurality of submodules comprises defining interfaces, data width, and the type of signal for one of the input lines and one of the output lines associated with one of the parameterized submodules.

14. (Currently amended) The method of claim [[6]] 33, wherein the submodules comprise adders, phase lock loops, memory, and timers.

15. (Currently amended) The method of claim [[6]] 9, wherein ~~generating one of the plurality of~~ one of the test designs further comprises ~~selecting~~ a clock structure for [[each]] one of the outputs.

16. (Currently amended) The method of claim 15, wherein the clock ~~structures include a plurality of~~ structure includes a synchronous and or an asynchronous ~~structures~~ structure.

17. (Canceled)

18. (Currently amended) The computer system of claim [[17]] 36, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip.

19. (Currently amended) The computer system of claim [[17]] 36, wherein the design automation tool is used to implement designs on an ASIC.

20. (Currently amended) The computer system of claim [[17]] 36, wherein the design automation tool is an electronic design automation tool.

21. (Currently amended) The computer system of claim [[17]] 36, wherein the design automation tool is a synthesis or a place and route tool.

22. (Canceled)

23. (Currently amended) The computer system of claim [[22]] 36, wherein said processor is configured to generate the one of the plurality of test designs by identifying a plurality of inputs, wherein the plurality of inputs ~~comprise~~ comprises the input pins of the top level module, one of the output lines of one of the parameterized submodules ~~output lines~~, and registers.

24. (Currently amended) The computer system of claim [[22]] 23, said processor is configured to generate the one of the plurality of test designs by identifying a plurality of outputs, wherein the outputs identified comprise the output pins of the top level module, one of the input lines of one of the parameterized submodules ~~input lines~~, and registers.

25. (Canceled)

26. (Currently amended) The apparatus of claim [[25]] 39, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip.

27. (Currently amended) The apparatus claim [[25]] 39, wherein the design automation tool is used to implement designs on an ASIC.

28. (Currently amended) The method of claim [[1]] 35, further comprising selecting a plurality of submodules upon said determining that the predetermined number of the test designs is not generated.

29-32. (Canceled)

33. (New) A method of generating a plurality of test designs associated with a design automation tool, the method comprising:

(a) instantiating an input/output (I/O) structure of a module having input and output pins;

(b) applying a function to select a plurality of submodules from a design module library, wherein the plurality of submodules comprises input and output lines;

(c) parameterizing the plurality of submodules from the design module library for interconnection with the module;

(d) interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types; and

(f) connecting the plurality of parameterized submodules to the input and output pins of the module.

34. (New) The method of claim 33, wherein the plurality of interconnect types include an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect.

35. (New) The method of claim 33, further comprising:

determining whether a predetermined number of the test designs for testing the design automation tool has been generated; and

applying the plurality of test designs to test the design automation tool.

36. (New) A computer system for generating a plurality of test designs associated with a design automation tool, the computer system comprising:

a memory operable to hold information associated with a design module library; and

a processor coupled to memory, wherein said processor is configured to:

(a) instantiate an input/output (I/O) structure of a module having input and output pins;

(b) apply a function to select a plurality of submodules from the design module library, wherein the plurality of submodules have s plurality of input and output lines;

(c) parameterizing the plurality of submodules from the design module library for interconnection with the module;

(d) interconnect the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types ; and

(e) connect the plurality of parameterized submodules to the input and output pins of the module.

37. (New) The computer system of claim 36, wherein the plurality of interconnect types include an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect.

38. (New) The computer system of claim 36, wherein the processor is configured to determine whether a predetermined number of the test designs for testing the design automation tool has been generated, wherein the plurality of test designs are applied to test the design automation tool.

39. (New) An apparatus for generating a plurality of test designs associated with a design automation tool, the apparatus comprising:

storage means for storing data design module library; and

processing means:

(a) for instantiating an input/output (I/O) structure of a module having input and output pins,

(b) for applying a function to select a plurality of submodules having input and output lines from the design module library,

(c) for parameterizing the plurality of submodules from the design module library for interconnection with the module,

(d) for interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types; and

(e) for connecting the plurality of parameterized submodules to the input and output pins of the module.

40. (New) The apparatus of claim 39, wherein said processing means:

(f) for determining whether a predetermined number of the test designs for testing the design automation tool has been generated, and

(g) for repeating selecting a plurality of submodules from the design module library upon determining that the predetermined number of test designs is not generated.

41. (New) The apparatus of claim 39, wherein the processing means for interconnecting the lines of the plurality of parameterized submodules based on the selection of the particular type of interconnect from the plurality of interconnect types including an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect.